REMARKS

This Amendment is submitted in response to the Office Action mailed January 25, 2006. Claims 1-4, 6, 7, 25-33, and 41-56 are presently pending and stand rejected.

Examiner objected to the specification. Assignee has amended to the specification and respectfully submits that the specification, as amended, overcomes Examiner's objection.

Claims 1-4, 6, 7 and 25-60 were rejected under 35 U.S.C. 112, first paragraph. Regarding claims 1-4, 6, 25, and 34-52, Examiner has indicated in the Office Action of June 14 ,2005 that:

> "In particular, Fig. 6 shows the implementation the device used to create the first clock frequency. The second clock frequency (C1) is input into feedback loop (block 601). However, the second clock frequency is generated at the output of an NCO (block 603), which is not a[ ]part of the feedback loop (block 601). There is no "looping" operation performed from the output of the NCO to the input of the feedback loop. Therefore, it would have been obvious to one skill[ed] in the art at the time the invention was made that the first clock frequency is not generated using a phase locked loop, rather the first clock frequency is generated using a feedback loop, half period calculator, and NCO, wherein the half-period calculator and NCO are separate from the feedback loop (the half period calculator and the NCO are not a[ ]part of the feedback loop)."

June 14, 2005, Office Action, at 3.

In the October 15, 2005 response, Applicant noted that "(1) The present application does enable one skilled in the art to make and use a "demultiplexer comprising a phase locked loop for generating the first clock frequency using said second clock frequency"; and "(2) Figure 6 enables one skilled in the art to make and use a "a phase locked loop for generating the first clock frequency using said second clock frequency". October 15, 2005 Response, pp. 10-11.

Examiner now responds that "In applicant's REMARKS applicant recites that Fig. 6 does in fact show 'a phase locked loop for generating the first clock frequency using said clock frequency'. However examiner asserts that Fig. 6 shows the implementation the device used to create the first clock frequency.

The second clock frequency (C1) is input into a feedback loop (block 601). However, the first clock frequency is generated at the output of an NCO (block 603), which is not apart from of the feedback loop (block 601)." Office Action, p.1.

However, Assignee also argued that, "For example, Examiner's attention is called to Application, Figure 5. In Figure 5, it can be seen that the phase lock loop (Digital PLL) generates first clock frequency, e.g. clock frequency F1, using second clock frequency, e.g., clock frequency C1. Although Examiner makes specific reference to Figure 6, it is respectfully noted that Figure 6 is 'a block diagram of one embodiment of the subsystems of PLL 52 illustrated in Fig. 5', in contrast to an exclusive embodiment. Application, Paragraph 41 (Emphasis Added). Therefore, even if Examiner's characterization of the embodiment described in Figure 6 were to be correct, the present application does teach one skilled in the art to make and use 'a phase locked loop for generating the first clock frequency using said second clock frequency', at the least, from Figure 5."

Assignee reasserts the foregoing argument.

Claims 1, 42, and 48 were rejected under 35 U.S.C. 102(b) as anticipated from Papas. Claims 26, 30, and 53 were rejected under 35 U.S.C. 103(a) as obvious from Papas in view of Kovacs, Hulsing, and/or Minoda. Assignee has amended claim 1 to include "generating the first clock frequency based at least in part on a number of audio pixels per line and said second clock frequency". Assignee respectfully submits neither Papas, Kovacs, Hulsing, or Minoda, alone, or in combination, teach or fairly suggest the foregoing. Claims 26, 30, 42, 48, and 53 are similarly amended.

Accordingly, Examiner is requested to withdraw the rejections under 102(b) and 103 to independent claims 26, 30, 42, 48, and 53 as well as to the dependent claims.

Conclusion

For at least the foregoing reasons, all of the pending claims are allowable. Should anything remain in order to place the present application in condition for

allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

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